(11)Publication number : 05-251432
(43)Date of publication of application : 28.09.1993

(51)Int.Cl. H01L 21/316
H01L 29/784

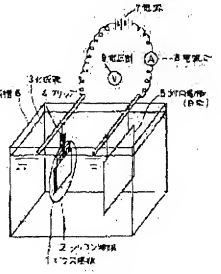
(21)Application number : 04-048536
(22)Date of filing : 05.03.1992

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : TSUTSU HIROSHI
SANO HIROSHI
FURUTA MAMORU
YOSHIOKA TATSUO
KAWAMURA TETSUYA
MIYATA YUTAKA

(54) METHOD FOR ANODIZING SILICON AND MANUFACTURE OF THIN FILM TRANSISTOR

(57)Abstract:
PURPOSE: To obtain an excellent anodic oxidization film with the clean boundary by using a formation liquid containing nitrate without alkali metals to anodize silicon.

CONSTITUTION: A formation liquid 3 obtained by dissolving ammonium nitrate of 0.04M in ethylene glycol, is pourod into a formation bath 6. A glass substrate 1 is immersed in the liquid 3, and pinched using a clip 4. The anodization current is fed from a power supply 7 through the clip 4. Using platinum 5 as opposed electrode 5 to the glass substrate, anodization is performed at a current density of 4-8mA/cm2 on a formation voltage of 150V to form an anodic oxidization film.



CLAIMS

[Claim(s)]
[Claim 1]transformation containing a nitrate which does not contain an alkaline metal for a semiconductor which uses silicon as the main ingredients — an anodization method of silicon anodizing using liquid and using the anodized film as a gate insulating layer.
[Claim 2]A silicon anodization method according to claim 1, wherein a nitrate which does not contain said alkaline metal contains ammonium nitrate (NH_4NO_3) or nitric acid tetramethylammonium ($[(CH_3)_4N]NO_3$) at least.

[Claim 3]The 1st process of forming a semiconductor layer selectively on a substrate, and the 2nd process of forming the 1st conductive layer so that said a part of semiconductor layer may be covered, and forming the 1st insulating layer in an exposed part of said semiconductor layer, The 3rd process of forming the 2nd conductive layer that removes said 1st conductive layer and serves as a gate electrode and gate bus wiring, The 4th process of introducing an impurity used as a donor or an acceptor, and forming the source region and a drain area into said semiconductor layer by using said 2nd conductive layer as a mask, The 5th process of carrying out covering formation of the 2nd insulating layer selectively, and the 6th process of forming the 3rd conductive layer selectively so that said sauce and a drain area may be contacted with source bus wiring and a source electrode and a drain electrode may be formed, A manufacturing method of a thin film transistor, wherein said semiconductor layer consists of a semiconductor which uses silicon as the main ingredients in a manufacturing method of a becoming thin film transistor, ** et al., even if small, and said 1st insulating layer anodizes and forms said semiconductor layer by supplying electric power from said 1st conductive layer.
[Claim 4]The 1st process of forming on a substrate the 1st semiconductor layer that hardly contains an impurity used as a donor or an acceptor, The 2nd process of forming the 2nd semiconductor layer containing an impurity used as a donor or an acceptor, The 3rd process of forming the 1st conductive layer selectively so that source bus wiring may be formed with sauce and a drain electrode, The 4th process of forming an insulating layer in an exposed part of said 2nd semiconductor layer, and the 5th process of forming the 2nd insulating layer selectively, In a manufacturing method of the 6th process of forming the 2nd conductive layer used as a gate electrode and gate bus wiring, and a thin film transistor, ** et al., which becomes even if small, A manufacturing method of a thin film transistor, wherein said semiconductor layer consists of a semiconductor which uses silicon as the main ingredients and said insulating layer anodizes and forms said semiconductor layer by supplying electric power from said 1st conductive layer.
[Claim 5]A manufacturing method of the thin film transistor according to claim 4, wherein said 2nd semiconductor layer carries out covering formation of the semiconductor layer containing an impurity on said 1st semiconductor layer selectively.
[Claim 6]A manufacturing method of the thin film transistor according to claim 4 forming said 2nd semiconductor layer by introducing an impurity into said 1st semiconductor layer.
[Claim 7]The 1st process of forming the 1st conductive layer used as source bus wiring, a source electrode, and a drain electrode on a substrate, The 2nd process of forming a semiconductor layer in an intersection of a transistor formation region and source bus wiring, and gate bus wiring selectively, The 3rd process of forming an insulating layer in an exposed part of said semiconductor layer, and an intersection of source bus wiring and gate bus wiring, In a manufacturing method of the 4th process of forming the 2nd conductive layer used as a gate electrode and gate bus wiring, and a thin film transistor, ** et al., which becomes even if small, A manufacturing method of a thin film transistor, wherein said semiconductor layer consists of a semiconductor which uses silicon as the main ingredients and said insulating layer anodizes and forms said semiconductor layer by supplying electric power from said 1st conductive layer.
[Claim 8]a substrate top — sauce and a drain electrode — with the 1st process of forming the 1st conductive layer selectively so that source bus wiring may also be formed, The 2nd process of forming the 1st semiconductor layer that hardly contains an impurity used as a donor or an acceptor, The 3rd process of forming the 2nd semiconductor layer containing an impurity used as a donor or an acceptor, The 4th process of forming an insulating layer in an exposed part of said 2nd semiconductor layer, and the 5th process of forming the 2nd insulating layer selectively.

In a manufacturing method of the 5th process of forming the 2nd conductive layer used as a gate electrode and gate bus wiring, and a thin film transistor, ** et al., which becomes even if small. A manufacturing method of a thin film transistor, wherein said semiconductor layer consists of a semiconductor which uses silicon as the main ingredients and said insulating layer anodizes and forms said semiconductor layer by supplying electric power from said 1st conductive layer.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the manufacturing method of a thin film transistor used for the anodization method of silicon and the semiconductor device which used the method, a display device, a photo detector, etc.
[0002]
[Description of the Prior Art]Since self-align art is possible for top gate type thin film transistors, such as a coplanar type, it is well used as transistor structure of various semiconductor devices. Here, it explains using the thin film transistor of the coplanar type using the polycrystalline silicon used as a part of drive circuit of a liquid crystal display as a semiconductor layer.
[0003]Drawing 7 shows the important section sectional view of the thin film transistor of the conventional coplanar type, 22 are an amorphous insulating substrate among a figure, a glass substrate, a quartz substrate, etc. are used, and the Si substrate occasionally covered by SiO_2 may be used. however, the glass substrate of low cost -- using -- about 600 ** or less,---- a process must be comparatively performed at low temperature. Here, it supposes that a low temperature process 600 ** or less is used, and a glass substrate is used as the amorphous insulating substrate 22.
[0004]On this glass substrate 22, Si_2H_6 is used as material gas, An amorphous silicon thin film is made to deposit with a low-pressure chemical vapor deposition method (below, it is written as the LP gas-CVD (Low Pressure-Chemical VaporDeposition) method) with a substrate temperature of 450 ** - 500 **. Since hydrogen is contained so much in the form of Si-H or Si-H_2 in this amorphous silicon thin film, heat treatment (300 ** - 450 **) is performed, and the hydrogen contained in said amorphous silicon thin film is desorbed.
[0005]Next, if low-temperature heat treatment (500 ** - 700 **) is performed for the amorphous silicon thin film by which hydrogen desorption was carried out and solid phase growth of said amorphous silicon thin film by which hydrogen desorption was carried out is carried out, the silicon thin film 23 which carried out solid phase growth, i.e., a polycrystalline silicon thin film, will grow. As an annealing atmosphere, nitrogen gas, hydrogen gas, argon gas, gaseous helium, etc. are used. Annealing may be performed in the high vacuum atmosphere of $1x10^{-6}$ to

$1x10^{-10}$Torr. In low-temperature annealing, only a crystal grain with the small crystal orientation of the activation energy of crystal growth grows selectively, and, moreover, it grows up greatly gently.

[0006]Next, said polycrystalline silicon thin film 23 is patterned after island shape by a general photolithography and etching. Next, a silicon oxide layer is formed as the gate insulating layer 24. There is the low-temperature method 500 ** or less like LP gas-CVD method, an optical-pumping CVD method or plasma CVD method, and an ECR plasma CVD method as a formation method of said gate insulating layer. When using a quartz substrate etc. as the amorphous insulating substrate 22, it can be based on a thermal oxidation method. Although there are a dry oxidation style and a wet oxidation style in this thermal oxidation method, although oxidizing temperature is as high as not less than 1000 **, since membraneous quality is excellent, the direction of the dry oxidation style is suitable.

[0007]Next, the gate electrode 25 is formed using polycrystalline silicon. As a method for film deposition, although there are methods, such as a CVD method and a sputtering technique, detailed explanation here is omitted. Then, the ion implantation of the impurity is carried out by using said gate electrode 25 as a mask, and the source region 26 and the drain area 27 are formed in self align. As said impurity, it is n Chillan. [0008]

[External Character 1]

ネル・トランジスタを作製する場合はP^+あるいはAs^+を用い、pチャンネル

・トランジスタを作製する場合はB^+等を用いる。不純物添加方法としては、

[0009]There are methods other than ion implantation, such as a laser doping process or the plasma doping method.

[0010]Then, as the layer insulation layer 28, a silicon nitride film (hundreds of nm - about several micrometers) is deposited, for example. As a formation method, LP gas-CVD method or plasma CVD method is easy. Mixed gas, such as SiH_4, NH_3, N_2, and H_2 gas, etc. are used for reactant gas.

[0011]Here, if a hydrogen ion is introduced by methods, such as a hydrogen plasma method, a hydrogen ion injection method, or a diffusion method of hydrogen from a plasma nitriding film, the defect of the dangling bond etc. which exist in a gate oxide interface etc. will be inactivated. Such a hydrogenation process may be performed before laminating the layer insulation layer 28.

[0012]Finally, the contact hole 29 is formed in said layer insulation layer 28 and the gate insulating layer 24, and it forms, using aluminum aluminum for example as the source electrode 30 and the drain electrode 31. Thus, a coplanar type thin film transistor is formed.

[0013]

[Problem(s) to be Solved by the Invention]However, in order to form the gate insulating layer 24 in the above-mentioned manufacturing method, When it is going to lower cost using the glass substrate 22 of low cost, formation of a gate insulating layer becomes formation and discontinuity of a semiconductor layer, a semiconductor / insulating-layer interface is polluted depending on the disposal method before gate insulating layer formation, and there is a problem referred to as degrading the characteristic of an element. If a quartz substrate is used, an oxidizing film can be used and a semiconductor / insulating-layer interface will be kept pure, but it has the problem that cost becomes high.

[0014]An object of this invention is to excel in the formation and performance of an insulating layer which keep a semiconductor / insulating-layer interface pure, and to provide the anodization method of the high silicon reliance, and the manufacturing method of a thin film transistor, using the glass substrate of low cost as a substrate in view of this point.

[0015]

[Means for Solving the Problem]transformation containing a nitrate which does not contain an alkaline metal for a semiconductor with which this invention uses silicon as the main ingredients -- it anodizes using liquid and this oxide film on anode is used as a gate insulating layer

[0016]

[Function]the transformation which contains the nitrate in which an alkaline metal is not

contained in this invention — liquid is used.
Therefore, it is a presentation almost equivalent to an oxidizing film, and moreover, into an oxide film on anode. reliability without movable ion is high and the good oxide film on anode of membraneous quality can be formed.

[0017]This invention can manufacture the thin film transistor which can hold a semiconductor layer / insulating-layer interface purely using the glass substrate of low cost not using a quartz substrate. The thin film transistor of this invention is a thin film transistor excellent in performance and reliability.
[0018]
[Example](Example 1) Drawing 1 shows the system schematic which enforces the anodization method of the 1st example of this invention, and this is the method of depositing the silicon thin film 2 on the glass substrate 1. This silicon may be any of single crystal silicon, polycrystalline silicon, and amorphous silicon. next, this glass substrate -- transformation -- the transformation which melted ammonium nitrate (NH_4NO_3) of 0.04M in the ECHIRE glycol filled in the tub 6 — it is immersed into the liquid 3, and inserts with the clip 4, and predetermined anodization current is supplied from the power supply 7 through this clip. Here, 8 is an ammeter, 9 is a voltmeter and the counterelectrode 5 is anodized using platinum with the current density 4 – 8 mA/cm^2, and the formation voltage 150V. Although based also on current density, an oxide film on anode about 100 nm thick is formed in 1 to 2 hours. According to measurement of ESCA (Electron Spectroscopy for Chemical Analysis), the presentation of this oxide film on anode is almost equivalent to an oxidizing film, and transformation -- since alkaline metals, such as potassium and sodium, are not contained in liquid, there is no movable ion into an oxide film on anode, and it is reliable. Since the dielectric breakdown electric field of this oxide film on anode has pressure-proofing sufficient as 8 MV/cm and a gate insulating layer, it can be used as a gate insulating layer.
[0019]the above-mentioned example — transformation -- although the solution which melted ammonium nitrate was used into ethylene glycol as the liquid 3 — nitric acid tetramethylammonium [$(CH_3)_4N$] If it is a nitrate which does not contain alkaline metals, such as NO_3, whatever it may use, an almost equivalent result is obtained.

[0020](Example 2) Drawing 2 shows the outline sectional view for every main process of the manufacturing method of the thin film transistor in the 2nd example of this invention, and first, as shown in drawing 2 (a), it carries out covering formation of the polycrystalline silicon 11 (semiconductor layer) selectively on the glass substrate 10. There is also the method of depositing polycrystalline silicon directly with methods, LP gas-CVD methods, etc., such as solid phase growth from amorphous silicon and laser annealing, in the covering formation of polycrystalline silicon.
[0021]Next, as shown in drawing 2 (b), the source electrode 12 and the drain electrode 13 are formed using aluminum aluminum. Although a graphic display is not carried out at this time, it forms so that electric power may be applied to both a source electrode, or both [either or] and it may be connected to the extraction electrode to the exterior.
[0022]Next, as shown in drawing 2 (c), aluminum is taken out by resist and is thoroughly covorod with the usual photo lithography except the polar zone. And the polycrystalline silicon 11 is anodized by the method of Example 1 the 1st invention shown in above-mentioned drawing 1. At this time, in order to increase the carrier density in a substrate face, it is desirable to perform an optical exposure.
[0023]Next, if the resist 14 is exfoliated, as shown in drawing 2 (d), the oxide film on anode 15 will be formed. Then, although a graphic display is not carried out, each source drain electrodes 12 and 13 are made to become independent by photo lithography etching once again. And for example, if the gate electrode 16 is formed using the chromium Cr, ion is driven in by using this gate electrode 16 as a mask and the source region 17 and the drain area 18 are formed, a thin film transistor as shown in drawing 2 (e) will be formed.
[0024](Example 3) Drawing 3 is an outline sectional view of the thin film transistor by the 3rd

example of this invention. The short defect by the pinhole in a gate insulating layer is reduced as a double gate insulating layer by laminating the layer insulation layers 19, such as silicon nitride, silicon oxide, and tantalum oxide, after oxide-film-on-anode formation (drawing 2 (c)) in Example 2.

[0025](Example 4) Drawing 4 shows the outline sectional view for every main process of the manufacturing method of the thin film transistor in the 4th example of this invention, and first carries out covering formation of the polycrystalline silicon 20 (semiconductor layer) which hardly contains an impurity on the glass substrate 10 as shown in drawing 4 (a). There is also the method of depositing polycrystalline silicon directly with methods, LP gas-CVD methods, etc., such as solid phase growth from amorphous silicon and laser annealing, in the covering formation of polycrystalline silicon. Next, the polycrystalline silicon 21 which contains many phosphorus as an impurity with LP gas-CVD method is deposited on this semiconductor layer, and it patterns by photo lithography etching like drawing 4 (a).

[0026]Next, the source electrode 12 and the drain electrode 13 are formed using aluminum aluminum like drawing 4 (b). Although a graphic display is not carried out at this time, it forms so that electric power may be applied to both a source electrode, or both [either or] and it may be connected to the extraction electrode to the exterior.

[0027]Next, aluminum is taken out by resist and is thoroughly covered with the usual photo lithography except the polar zone. And the polycrystalline silicon 21 containing many phosphorus is anodized by the method of Example 1. At this time, in order to increase the carrier density in a substrate face, it is desirable to perform an optical exposure. Anodizing becomes easy [since the process of impurity ion placing for forming the source drain areas 17 and 18 (refer to drawing 2) not only becomes unnecessary, but the polycrystalline silicon 21 containing many phosphorus is used as silicon which performs anodization according to this method, conductivity is high and].

[0028]Next, if resist is exfoliated, as shown in drawing 4 (c), the oxide film on anode 15 will be formed. Then, although a graphic display is not carried out, each source drain electrodes 12 and 13 are made to become independent by photo lithography etching once again.

[0029]And it becomes possible by laminating polycrystalline silicon on the whole surface, for example, applying negative resist to the whole surface, and exposing from a rear face for gate electrode formation, to form the gate electrode 16 in self-align after depositing the insulating layer 19 between groups. Thus, a thin film transistor as shown in drawing 4 (d) is formed.

[0030]Although the polycrystalline silicon which contains many phosphorus using LP gas-CVD method was deposited in the above-mentioned example, methods, such as the other methods, for example, plasma CVD method, a sputtering technique, and an ECR-CVD method, may be used. Although the polycrystalline silicon containing many phosphorus was used as an impurity, anything may be sufficient as long as it is an impurity used as donors, such as arsenic and boron, or an acceptor.

[0031]Although the gate electrode was formed in self-align in the above-mentioned example, it cannot be overemphasized that it may form by the usual photo lithography etching.

[0032](Example 5) This example introduces the ion used as the impurity which serves as a donor or an acceptor near the surface of the polycrystalline silicon which hardly contains an impurity in Example 4 by methods, such as ion implantation, a plasma dope, and an ion shower dope. The semiconductor layer containing an impurity is formed and a graphic display in particular is not carried out.

[0033](Example 6) Drawing 5 shows the outline sectional view for every main process of the manufacturing method of the thin film transistor in the 6th example of this invention, and first carries out covering formation of the polycrystalline silicon 20 (semiconductor layer) which hardly contains an impurity on the glass substrate 10 as shown in drawing 5 (a) selectively. There is also the method of depositing polycrystalline silicon directly with methods, LP gas-CVD methods, etc., such as solid phase growth from amorphous silicon and laser annealing, in the covering formation of this polycrystalline silicon 20.

[0034]Next, on this semiconductor layer, the polycrystalline silicon 21 which contains many phosphorus as an impurity with LP gas-CVD method is deposited, and it patterns by photo

lithography etching. And if the source drain electrodes 12 and 13 are formed, for example using aluminum aluminum, drawing 5 (a) will be obtained. Although a graphic display is not carried out at this time, it forms so that electric power may be applied to both a source electrode, or both [either or] and it may be connected to the extraction electrode to the exterior.

[0035]Next, as shown in drawing 5 (b), aluminum is taken out by the resist 14 and is thoroughly covered with the usual photo lithography except the polar zone. And the polycrystalline silicon 21 containing many phosphorus is anodized by the method of Example 1. At this time, in order to increase the carrier density in a substrate face, it is desirable to perform an optical exposure. Anodizing becomes easy [since the process of impurity ion placing for forming the source drain areas 17 and 18 (refer to drawing 2) not only becomes unnecessary according to this method, but the polycrystalline silicon 21 containing many phosphorus is used as silicon which performs anodization, conductivity is high, and].

[0036]Next, if resist is exfoliated, as shown in drawing 5 (c), the oxide film on anode 15 will be formed. Then, although a graphic display is not carried out, each source drain electrodes 12 and 13 are made to become independent by photo lithography etching once again.

[0037]Finally, if the chromium Cr is used for formation of the gate electrode 16, for example and it forms, a thin film transistor as shown in drawing 5 (d) will be formed.

[0038]Although the polycrystalline silicon which contains many phosphorus using LP gas-CVD method was deposited in the above-mentioned example, methods, such as the other methods, for example, plasma CVD method, a sputtering technique, and an ECR-CVD method, may be used. Although the silicon containing many phosphorus was used as an impurity, anything may be sufficient as long as it is an impurity used as donors, such as arsenic and boron, or an acceptor.

[0039](Example 7) Drawing 6 shows the outline sectional view for every main process of the manufacturing method of the thin film transistor in the 7th example of this invention, and first, as shown in drawing 6 (a), it forms the source electrode 12 and the drain electrode 13 using the glass substrate 10 top, for example, aluminum aluminum. Although a graphic display is not carried out at this time, it forms so that electric power may be applied to both a source electrode, or both [either or] and it may be connected to the extraction electrode to the exterior. And covering formation of the polycrystalline silicon 20 (semiconductor layer) which hardly contains an impurity is carried out selectively. There is also the method of depositing polycrystalline silicon directly with methods, LP gas-CVD methods, etc., such as solid phase growth from amorphous silicon and laser annealing, in the covering formation of polycrystalline silicon. Next, the polycrystalline silicon 21 which contains many phosphorus as an impurity, for example with LP gas-CVD method is deposited, and it patterns by photo lithography etching like drawing 6 (a).

[0040]And next, as shown in drawing 6 (b), aluminum is taken out by the resist 14 and is thoroughly covered with the usual photo lithography except the polar zone. And the polycrystalline silicon 21 containing many phosphorus is anodized by the method of Example 1. At this time, in order to increase the carrier density in a substrate face, it is desirable to perform an optical exposure. Anodizing becomes easy [since the process of impurity ion placing for forming the source drain areas 17 and 18 (refer to drawing 2) not only becomes unnecessary, but the polycrystalline silicon containing many phosphorus is used as silicon which performs anodization according to this method, conductivity is high, and].

[0041]Next, if resist is exfoliated, a graphic display will not be carried out after that in which the oxide film on anode 15 as shown in drawing 6 (c) is formed, but each source drain electrodes 12 and 13 are made to become independent by photo lithography etching once again.

[0042]If the layer insulation layer 19 is finally deposited and it forms, chromium-Cr-using the gate electrode 16 for example, a thin film transistor as shown in drawing 6 (d) will be formed.

[0043]In the above-mentioned example, an order of the formation process of a source drain electrode and the formation process of the polycrystalline silicon which does not contain an impurity may be replaced.

[0044]Although the polycrystalline silicon which contains many phosphorus using LP gas-CVD method was deposited in the above-mentioned example, methods, such as the other methods, for example, plasma CVD method, a sputtering technique, and an ECR-CVD method, may be

used. Although the polycrystalline silicon containing many phosphorus was used as an impurity, anything may be sufficient as long as it is an impurity used as donors, such as arsenic and boron, or an acceptor.

[0045]Although the gate electrode was formed in self align in the above-mentioned example, it cannot be overemphasized that it may form by the usual photo lithography etching.

[0046]

[Effect of the Invention]as explained above, in this invention, it is a presentation almost equivalent to an oxidizing film --- moreover -- transformation --- alkaline metals, such as potassium and sodium, are not contained in liquid.

Therefore, there is no movable ion into an oxide film on anode, it is reliable and the dielectric breakdown electric field can form an oxide film on anode with pressure-proofing sufficient as 8 MV/cm and a gate insulating layer.

[0047]According to this invention, the thin film transistor which can be held purely can manufacture a semiconductor layer / insulating-layer interface by low cost. The thin film transistor of this invention is a thin film transistor excellent in performance and reliability, and the practical effect is large.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is the system schematic which enforces the anodization method in Example 1 of this invention.

[Drawing 2]It is an outline sectional view for every main process of the manufacturing method of the thin film transistor in Example 2 of this invention.

[Drawing 3]It is an outline sectional view of the thin film transistor manufactured by the manufacturing method of the thin film transistor in Example 3 of this invention.

[Drawing 4]It is an outline sectional view for every main process of the manufacturing method of the thin film transistor in Example 4 of this invention.

[Drawing 5]It is an outline sectional view for every main process of the manufacturing method of the thin film transistor in Example 6 of this invention.

[Drawing 6]It is an outline sectional view for every main process of the manufacturing method of the thin film transistor in Example 7 of this invention.

[Drawing 7]It is an important section sectional view of the manufactured coplanar type thin film transistor by the conventional method.

[Description of Notations]

1 and 10 --- a glass substrate and 2 --- a silicon thin film and 3 -- transformation -- Liquid and 4 --- [and] 5 --- a counterelectrode (platinum) and 6 --- transformation --- A tub and 7 --- a power supply and 8 --- an ammeter, 9 [--- Drain electrode,] --- A voltmeter and 11 --- Polycrystalline silicon, 12 --- A source electrode and 13 14 [--- The source region and 18 / --- A drain area and

19 / --- A layer insulation layer and 20 / -- The polycrystalline silicon, 21 which hardly contain an impurity / -- Polycrystalline silicon containing many phosphorus] --- Resist and 15 --- An oxide film on anode and 16 --- A gate electrode, 17

[Translation done.]

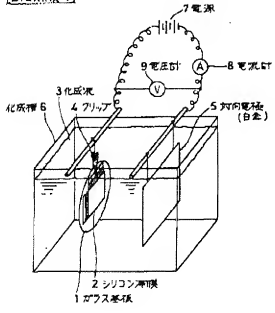
* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

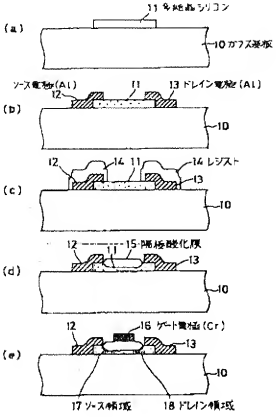
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

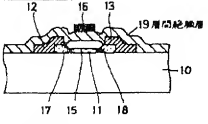
[Drawing 1]



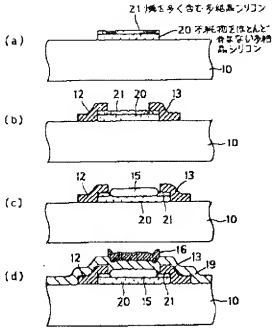
[Drawing 2]



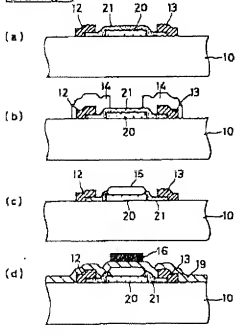
[Drawing 3]



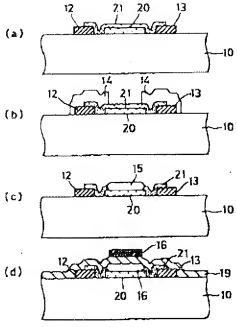
[Drawing 4]



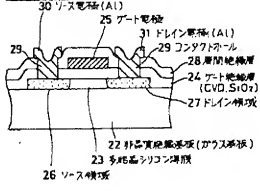
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Translation done.]